

**SYSTEM AND METHOD FOR INTEGRATION OF HfO₂
AND RTCVD POLY-SILICON**

Inventors: Yu Min Lin
6F.-3, No.429, Yanping Rd., Jhongli City
Taoyuan County, Taiwan 320, Republic of China
Citizenship: Taiwan, R.O.C.

Ming-Fang Wang
No.327, Jhongping Rd., Shengang Township
Taichung County, Taiwan 429, Republic of China
Citizenship: Taiwan, R.O.C.

Kun-Chih Lee
No.2, Cyuansing Village, Sinhua Township
Tainan County, Taiwan 712, Republic of China
Citizenship: Taiwan, R.O.C.

Ming-Ho Yang
9F., No.72-9, Lane 531, Sec. 1, Guangfu Rd.
Hsin-Chu, Taiwan 300, Republic of China
Citizenship: Taiwan, R.O.C.

Liang-Gi Yao
No. 6, Alley 1, Lane 158
Chang Chuen Street
Hsin-Chu, Taiwan 300, Republic of China
Citizenship: Taiwan, R.O.C.

Shih-Chang Chen
5F.-A, No.970, Sec. 4, Jhongsing Rd., Jhudong Township
Hsinchu County, Taiwan 310, Republic of China
Citizenship: Taiwan, R.O.C.

Assignee: Taiwan Semiconductor Manufacturing Co., Ltd.
No. 8, Li-Hsin Rd. 6, Science-Based Industrial Park
Hsin-Chu, Taiwan 300-77, R.O.C.

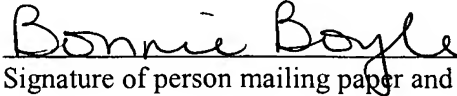
HAYNES AND BOONE, LLP
901 Main Street, Suite 3100
Dallas, Texas 75202-3789
(214) 651-5000
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BACKGROUND

[0001] The present disclosure relates generally to the field of semiconductor processing and, more particularly, to a method and system for improving electrical characteristics of dielectrics having a high dielectric constant.

[0002] An integrated circuit (IC) is formed by creating one or more devices (e.g., circuit components) on a semiconductor substrate using a fabrication process. As fabrication processes and materials improve, semiconductor device geometries have continued to decrease in size since such devices were first introduced several decades ago. For example, current fabrication processes are producing devices having geometry sizes (e.g., the smallest component (or line) that may be created using the process) of less than 0.1 μm . However, the reduction in size of device geometries frequently introduces new challenges that need to be overcome.

[0003] As semiconductor devices, such as metal oxide semiconductor field effect transistors (MOSFETs), are scaled below 0.1 μm , ultra thin SiO₂ gate oxide dielectric films that form portions of the devices may exhibit undesirable leakage current. In order to minimize leakage current while maintaining high drive current, high equivalent oxide thickness (EOT) may be achieved by using thinner films with higher dielectric constants (k). EOT is a thickness value used to compare the performance of MOS gate dielectrics having a dielectric constant that is different than SiO₂ with the performance of SiO₂ MOS gate dielectrics. For example, EOT may be used to represent the SiO₂ gate oxide thickness required to obtain the same gate capacitance as would be obtained with the alternate dielectric featuring the different dielectric constant k. One

method of reducing the EOT is by placing a high-k dielectric film (a film having a dielectric constant k greater than that of SiO_2) immediately over the gate of a MOSFET or over the area where the high-k dielectric becomes the gate of a MOSFET. However, high-k dielectric films may not have the desired electrical properties needed for a particular device design, and therefore, post processing may be necessary. Such post processing adds complexity to the fabrication process and increases production time and costs.

[0004] Accordingly, what is needed in the art is a integrated circuit device and method thereof that addresses the above discussed issues.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] Fig. 1A illustrates a method for integrating transistor gate deposition processes to produce a semiconductor device having improved electrical characteristics.

[0007] Fig. 1B illustrates a schematic view of one embodiment of a process reactor for providing a loading treatment constructed according to aspects of the present disclosure.

[0008] Figs. 2A-2D are cross-sectional views of an exemplary integrated circuit produced by a fabrication process that utilizes the method of Fig. 1.

DETAILED DESCRIPTION

[0009] It is understood that the following disclosure provides many different embodiments or examples. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0010] Referring to Fig. 1A and with additional reference to Figs. 2A-2D, in one embodiment, a method 100 illustrates a portion of a fabrication process that may be used to

produce a semiconductor device, such as a metal oxide semiconductor (MOS) device. It is understood that the MOS device may be a positive-channel MOS (PMOS) structure or a negative-channel MOS (NMOS) structure, and may have a single finger design or a multiple finger design. In the present example, the method 100 is used in the fabrication of a gate on the MOS device.

[0011] The method 100 may begin after other fabrication steps have been completed. For example, referring to Fig. 2A, prior to the start of the method 100, formation of a device 200 may have commenced over or on a substrate 202. The substrate 202 may comprise silicon, silicon-on-insulator (SOI), and/or diamond. The substrate 202 may be n-type doped or p-type doped, and is n-type doped in the present example for purposes of illustration. The substrate 202 may be provided with one or more isolation features (not shown). The isolation features may comprise local oxidation of silicon (LOCOS) structures and/or shallow trench isolation (STI) structures that are formed in the substrate 202 to electrically isolate device areas.

[0012] A well region 204 may be formed in the substrate 202 by ion implantation (although use of a p-type doped substrate may negate the need for a well region). For example, the well region 204 may be formed by growing a sacrificial oxide on the substrate 202, opening a pattern for the location of the well, and then using a chained-implantation procedure. It is understood that the substrate 202 may have a p-type doped well, an n-type doped well, and/or a combination thereof. While not limited to any particular dopant types or schemes, in one embodiment, the well region 204 may employ boron as a p-type dopant and deuterium-boron complexes for an n-type dopant. The deuterium-boron complexes may be formed by plasma treatment of boron-doped diamond layers with a deuterium plasma.

[0013] In one embodiment, the well region 204 may be formed using a high density plasma source with a carbon-to-deuterium ratio ranging between about 0.1 percent and about 5 percent in a vacuum process ambient. Boron doping may be provided by the mixing of a boron containing gas with a carbon/hydrogen gas. The boron containing gas may include B_2H_6 , B_2D_6 , and/or other boron containing gases. The concentration of boron doping may depend upon the amount of boron containing gas that may be leaked or added into the process. The process ambient pressure may range between about 0.1 mTorr and about 500 Torr. The substrate 202 may be held at a temperature ranging between about 150°C and about 1100°C. High density plasma may be produced by a microwave electron cyclotron resonance (ECR) plasma, a helicon

plasma, an inductively coupled plasma, and/or other high density plasma sources. For example, the ECR plasma may utilize microwave powers ranging between about 800 Watts and about 2500 Watts.

[0014] As described above, the well region 204 may also comprise n-type deuterium-boron complex regions of the substrate 202, which may be formed by treating the above-described boron-doped regions employing a deuterium plasma. For example, selected areas of the substrate 202 may be covered by photoresist or another type of mask such that exposed boron-doped regions may be treated with the deuterium containing plasma. The deuterium ions may provide termination of dangling bonds, thereby transmuting the p-type boron-doped regions into n-type deuterium-boron complex regions. Alternatively, deuterium may be replaced with tritium, hydrogen and/or other hydrogen containing gases. The concentration of the n-type regions may generally be controlled by a direct current (DC) or a radio frequency (RF) bias of the substrate 202. The above-described processes may also be employed to form lightly-doped source/drain regions in the substrate 202. Of course, other conventional and/or future-developed processes may also or alternatively be employed to form the source/drain regions.

[0015] Referring again to Fig. 1A, the method 100 begins in step 102 with the cleaning of the substrate 202 (Fig. 2A). The substrate 202 may be cleaned using one or more chemical cleaners and cleaning methods. For example, the chemical cleaner may be a mixture of H_2SO_4 and H_2O_2 (commonly known as sulfuric peroxide mix (SPM)) that may be used for removing native oxides. Other exemplary chemical cleaners and cleaning methods include a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionized (DI) water, commonly referred to as an "SC1 clean," as well as a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2), and deionized (DI) water, commonly referred to as an "SC2 clean." The chemical cleaning may be carried out in an high vacuum environment to prevent the formation of an ultra thin oxide that may occur if the substrate 202 is cleaned in an ambient environment.

[0016] In step 103 of Fig. 1A and with additional reference to Fig. 2A, a thin insulate 205 may optionally be deposited or formed over or on the cleaned substrate 202. The thin insulate 205 may be formed by a plurality of different methods. For example, the thin insulate 205 may be formed upon exposure to air wherein about 3 Angstroms to about 15 Angstroms of native

oxide may form on the semiconductor substrate 202. Alternatively, the cleaned substrate 202 may proceed to a process where the thin insulate 205 of SiO₂ may be formed by a low temperature RTP or thermal process. The transfer to the process for forming the thin insulate 205 may be under an inert gas or vacuum environment. Formation of the thin insulate 205 may include an Ar plasma clean prior to the growth of the thin insulate 205. Native oxide may be cleaned from the substrate 202 by the plasma clean and the thin insulate 205 may be deposited insitu of the plasma clean. The thin insulate 205 may comprise a variety of different materials including SiO₂, SiC, CN, and SiOC. The thin insulate 205 may be used as a MOS gate oxide, and may be a thermal oxide, carbon nitride, or any other appropriate gate dielectric film. In some examples, the thin insulate 205 may be too thin to be of any appreciable significance, and in other examples, it may be formed so as to have a thickness suitable for a gate oxide.

[0017] In step 104 of Fig. 1A and with additional reference to Fig. 2B, a dielectric layer 206 is deposited on or over the thin insulate 205 and/or the cleaned substrate 202. The layer 206 may comprise a high-k dielectric material, such as TaN, TiN, Ta₂O₅, HfO₂, ZrO₂, HfSiON, HfSi_x, HfSi_xN_y, HfAlO₂, NiSi_x, and/or other suitable materials, and may be formed by atomic layer deposition (ALD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), evaporation, and/or other methods. Generally, the layer 206 may have a thickness between ranging between about 3 Angstroms and about 50 Angstroms. With some materials, such as HfO₂, the layer 206 may be blanket deposited on or over the substrate 202, while other materials may be selectively deposited. Alternatively, it may be desirable to blanket deposit some materials, including HfO₂, in some fabrication processes, while selectively depositing the same materials in other processes.

[0018] In the present example, HfO₂ is to be deposited as the layer 206 using ALD, which may provide good step coverage, even on large areas, and a dense and pinhole free structure. ALD may be particularly useful for the deposition of metals and metal oxides in high packing density and/or high aspect ratio applications which have relatively demanding thin film requirements. In ALD, films grow with a relatively constant growth rate, and each deposition cycle ideally produces one molecular layer of the deposited material on the substrate surface. Usually, however, the growth rate is below one molecular layer per cycle because the absorbed source chemical molecules may be bulky or the substrate temperature may affect the number of active sites (e.g., -OH groups) on the substrate surface. Metal oxide thin films produced by

ALD are generally uniform and have desirable adhesion properties that allow them to become firmly bonded to the substrate surface.

[0019] The ALD of a high-k material, such as HfO_2 , may be achieved by co-reacting a precursor in the presence of a gas, and then purging the precursor using the same gas. For HfO_2 , ALD may utilize a precursor of Hf, such as HfCl_4 , or other organometallic Hf sources having a variety of ligands attached to the Hf atom may be utilized. For example, appropriate precursors may include HfCl_4 or $\text{Hf}(\text{OR})_4$, where R is an alkyl such as $\text{CH}(\text{CH}_3)_2$; $\text{Hf}(\text{tmdh})_4$, where tmdh = 2,2,6,6-tetramethyl-3,5-heptanedionato; $\text{Hf}(\text{tfac})_4$, where tfac = trifluoroacetylacetonate; or $\text{Hf}(\text{NO}_3)_4$. Similar precursors may be used for the ALD of other high-k materials, such as ZrO_2 . Because carbon containing hafnium precursors may result in excess carbon and fluorine incorporation in the metal oxide film, HfCl_4 may be desirable because it may result in limited residual chlorine incorporation. HfCl_4 may also be a preferred metal oxide precursor because it may be sublimated by injection and vaporization into the process reactor.

[0020] H_2O vapor may be selected as an oxygen source for the HfO_2 . In the present example, an HfO_2 deposition process may be carried out at a temperature ranging between about 200°C and about 400°C , such as about 300°C , with a deposited film thickness ranging between about 3 Angstroms and about 75 Angstroms, such as about 35 Angstroms. The ALD process may be performed in cycles with a series of HfO_2 monolayers formed during each cycle until the desired film thickness is achieved for the layer 206.

[0021] In step 106 of Fig. 1A and with continued reference to Fig. 2B, a first anneal may be performed on the substrate 202 after the deposition of the layer 206. Although the first anneal may be selected from a variety of anneals, in the present example the first anneal is a hydrogen-based anneal treatment. The hydrogen-based anneal treatment may cause hydrogen (H_2) to attach to any residual chlorine (Cl) that may be in the upper monolayers of the layer 206. The resulting effluent HCl may then be driven out of the substrate 202. Accordingly, the hydrogen-based anneal may aid in reducing interface traps on the surface of the layer 206. In the present example, the hydrogen-based anneal is performed using H_2 , but other gases containing hydrogen, such as NH_3 and SiH_4 , may also be used in the first anneal.

[0022] For purposes of illustration, the hydrogen-based anneal may be performed at a temperature between ranging between about 500°C and about 1000°C , and at a pressure ranging between about 0.1 Torr and about 760 Torr, or, in one embodiment, between about 10

Torr and about 70 Torr. The processing time for the hydrogen anneal may range between about 10 seconds and about 10 minutes. In the present example, the hydrogen-based anneal is performed for about one minute at a temperature of about 800° C and a pressure of about 40 Torr. The hydrogen-based anneal may be performed in a rapid thermal process (RTP), in which a single semiconductor substrate may be quickly treated. The hydrogen-based anneal may also be carried out in a conventional furnace where multiple semiconductor substrates are treated in a batch.

[0023] In step 108 of Fig. 1A and with continued reference to Fig. 2B, a second anneal may be performed on the layer 206. Although the second anneal may be selected from a variety of anneals, in the present example the second anneal is an oxygen-based anneal treatment. The second anneal may be a diluted oxygen anneal (DOA) performed in the presence of oxygen (O_2) or other oxygen sources, such as N_2O , NO , or D_2O . The oxygen-based anneal may be used following the hydrogen-based anneal of step 106 to improve the electrical characteristics of the layer 206 (and the resulting MOS gate). In one embodiment, the second anneal is performed at a temperature ranging between about 700° C and about 900° C, and at a pressure ranging between about 1 milliTorr and about 10 Torr. The processing time for the oxygen-based anneal may range between about 1 second and about 60 minutes, and may be selected to support RTP. In the present example, the oxygen-based anneal is performed for about 1 to about 300 seconds at a temperature of about 700° C to about 900° C and a pressure of about 0.1 Torr to about 10 Torr.

[0024] Typically, the use of high-k materials, such as HfO_2 , in a MOS gate formation process increases the density of interface traps which causes a flatband voltage shift and a more "stretched out" capacitance-gate voltage (CV) curve. Interface traps may form at sites of imperfect interfaces between the semiconductor substrate and the high-k material. For example, dangling bonds may trap electrons and interfere with the operations performed by electrons that travel through the gate structure.

[0025] A related problem associated with the deposition of HfO_2 is that the chlorine contamination of the HfO_2 film may reduce the insulating characteristics of the film and increase leakage. Secondary ion mass spectrometry (SIMS) depth profile analysis of hydrogen treated HfO_2 surfaces has shown that the hydrogen-based anneal treatment may drive a significant amount of Cl out of the HfO_2 film from a depth of up to about 3 nm. The Cl content reduction in

the HfO₂ film may reduce the flatband voltage and improve electron and hole mobility in the gate structure.

[0026] In step 110 of Fig. 1A and with reference to Fig. 2C, a loading treatment may be applied to the layer 206 and the substrate 202. Prior to steps that may follow step 106, the surface of the layer 206 and the substrate 202 may have a plurality of dangling (-OH) bonds. The dangling bonds may have a negative impact upon any proceeding process after any of the preceding steps 102-108. Step 110 optionally applies a loading treatment that may be applied prior to the commencement of the deposition of a polysilicon layer 208. The loading treatment may be performed insitu (within the same process environment) or exsitu (within an individual process) of the polysilicon layer 208 deposition process. The loading treatment may consist of a H₂ gas treatment, wherein the gas may be passed across the substrate 202. Alternatively, the loading treatment may include NH₃, SiH₄, and/or other gases. The substrate 202 may be heated by a rapid thermal chemical vapor deposition (RTCVD) reactor.

[0027] Referring to Fig. 1B and with continued reference to Fig. 2C, in one embodiment the loading treatment may comprise the periodic H₂ gas treatment of a pseudo-substrate 122 in a process chamber 120. The process chamber 120 may provide single substrate processing of the substrate 202 and a pseudo-substrate 122. The process chamber 120 may provide for CVD, PECVD, ALD, and/or other processes. The process chamber 120 may comprise a single or multiple substrate 202 and/or pseudo-substrate 122. The pseudo-substrate 122 may comprise Si, SiN, SiGe, diamond, ceramic, SiC, and/or other materials. The pseudo-substrate 122 may be periodically placed into the process chamber 120, and the loading treatment may be applied to the pseudo-substrate 122. The H₂ gas treatment of the pseudo-substrate 122 may be carried out at a temperature ranging between about 550° C and about 750° C. The H₂ gas loading treatment of the pseudo-substrate 122 may have a process time ranging between about 1 second and about 5 minutes. The H₂ gas employed during the loading treatment may also be excited by a plasma source. The process chamber 120 may have a process environment pressure ranging between about 0.1 Torr and about 80 Torr.

[0028] Following the loading treatment, the pseudo-substrate 122 may be removed from the process chamber 120 and the substrate 202 may be placed into the process chamber 120. The pseudo-substrate 122 may be subsequently placed into the process chamber 120 and treated with the H₂ gas loading treatment at periodic intervals. For example, the pseudo-substrate 122 may be

processed by the loading treatment sequentially after the processing of the substrate 202.

Alternatively, the pseudo-substrate 122 may be processed by the loading treatment at greater intervals between processing of the substrate 202. The interval may, for example, comprise five, twelve, or twenty-four substrates 202.

[0029] The substrate 202 may be treated in the same process chamber used by later step 112. The substrate 202 may be heated at a loading temperature ranging between about 450° C and about 650° C, possibly at about 625° C. The loading treatment step 208 process time may range between about 1 second and about 5 minutes, possibly at about 60 seconds. The partial pressure of the H₂ gas may range between about 20 Torr and about 80 Torr during step 110 of the loading treatment, possibly about 40 Torr.

[0030] At step 112 of Fig. 1A and with reference to Fig. 2C, a polysilicon layer 208 may be deposited on or over the treated layer 206 and the substrate 202, and the poly-silicon layer 208, layer 206, and possibly insulate 205 may be etched or otherwise patterned to at least partially form a poly-silicon gate structure. The poly-silicon layer 208 may be deposited using a process such as low pressure chemical vapor deposition (LPCVD) or ALD upon the layer 206 and the substrate 202 in a single or batch substrate reactor, and may be heated by infra-red (IR) lamps, resistive elements, and/or other sources. The substrate 202 may be heated at a loading temperature ranging between about 550° C and about 900° C, possibly at about 600° C. The step 112 process time may range between about 1 second and about 20 minutes, such as about 60 seconds. The pressure of the process chamber may range between about 1 milliTorr and about 760 Torr during step 112, such as about 60 milliTorr.

[0031] It is understood that additional processing steps may occur between step 102 and step 112. For example, the semiconductor substrate may be moved to a different location, or a chamber in which the first anneal is performed may be evacuated to prepare the chamber for another anneal or treatment. Moreover, while an annealing process is used for purposes of example at steps 106 and 108, it is understood that other treatments may be used instead. Accordingly, additional and/or alternative treatments may be performed on the layer 206, and such treatments include, but are not limited to, other types and/or processing conditions of annealing processes. For example, a treatment may be performed at a lower temperature than may be needed for an annealing process.

[0032] Referring now to Fig. 2D, illustrated is a sectional view of the device 200 shown in Fig. 2C in a subsequent stage of manufacture, in which a silicide layer 210 may be deposited onto or over the polysilicon layer 208. The silicide layer 210 may be a metal silicide using one or more metals such as titanium, tungsten, cobalt, and/or nickel. Source and drain extensions (SDEs) 212, 214 (e.g., lightly P- doped areas for a source and drain) in the substrate 202 may also be formed, such as by low energy implantation. Spacers 216 may then be formed, such as by LPCVD and/or other processes. The spacers 216 may comprise an insulating material such as silicon nitride or silicon oxide. The deposited insulating material may then be etched to form the spacers 216. Heavy p-type doped source and drain regions 218, 220, respectively, may then be formed, such as by ion implantation. A rapid thermal annealing (RTA) step may be used to activate the implanted dopants. In some embodiments, the source 218 may be connected to a n-type doped guard ring 222 which may be grounded.

[0033] Thus, the present disclosure introduces a method for fabricating a portion of an integrated circuit on a semiconductor substrate. In one embodiment, the method includes cleaning the surface of the substrate and forming a thin insulate over the substrate. The method also includes depositing a high dielectric constant (high-k) material over the thin insulate, and then performing a hydrogen-based anneal on the high-k material. The method further includes performing an oxygen-based anneal on the high-k material, wherein the hydrogen-based and oxygen-based anneals occur sequentially.

[0034] Another embodiment of a method for fabricating a portion of an integrated circuit on a semiconductor substrate is also disclosed herein. Such an embodiment includes placing a pseudo-substrate in a process reactor and applying a loading treatment to the pseudo-substrate. The method further includes removing the pseudo-substrate from the process reactor, placing a device substrate into the process reactor, and forming a poly-silicon layer upon the device substrate.

[0035] The present disclosure also provides another method for fabricating a portion of an integrated circuit on a semiconductor substrate. In one embodiment, the method includes cleaning the surface of the substrate; forming a thin insulate on the substrate, and depositing a high dielectric constant (high-k) material upon the thin insulate. An anneal is performed on the high-k material, and a loading treatment is applied upon the high-k material. A poly-silicon

layer is formed on the treated high-k material, wherein the anneal and poly-silicon deposition occur sequentially.

[0036] A microelectronic device is also introduced in the present disclosure. In one embodiment, the microelectronic device includes a doped well located in a substrate and a gate structure located over the substrate. The gate structure includes a dielectric layer located over the doped well, and a semiconductor layer located over the dielectric layer, wherein the dielectric layer is sequentially treated with a first, hydrogen-based anneal and a second, oxygen-based anneal. The microelectronic device also includes source/drain regions located in the doped well on opposing sides of the gate structure and extending partially between the dielectric layer and the doped well.

[0037] While the disclosure has been particularly shown and described with reference to exemplary embodiments, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the disclosure. For example, various parameters may be altered with respect to the chemical(s) selected for a treatment, as well as processing conditions (e.g., temperature, pressure, time, etc.). In addition, while the present disclosure uses a MOS device for purposes of illustration, it is understood that the present disclosure is equally applicable to dynamic random access memory (DRAM) devices, magnetoresistive RAM (MRAM) devices, capacitors, and other devices that may be fabricated on a semiconductor substrate using a high-k dielectric layer.